

AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated below. The language being added is underlined ("__") and the language being deleted contains either a strikethrough ("—") or is enclosed by double brackets ("[[]]").

1-34. (Canceled).

35. (Currently Amended) A method for preventing a DC flow condition caused by a transmit signal, comprising:

determining whether a data signal exhibits a change in value based on an asynchronous counter and a predetermined limit, wherein while monitoring the data signal, the asynchronous counter is updated or reset based on whether the data signal maintains a current logic level for multiple clock cycles;

generating a first signal in response to determining that the data signal does not exhibit a change in value to prevent the DC flow condition;

monitoring a clock signal; and

generating a second signal in response to a clock signal condition to prevent the DC flow condition.

36. (Original) The method of claim 35, wherein the data signal is provided by a delta-sigma modulator.

37. (Canceled)

38. (Original) The method of claim 35, wherein the first signal is a power down signal.

39. (Canceled)

40. (Currently Amended) The method of claim [[39]] 38, wherein the power down signal is generated by an asynchronous counter that reaches a maximum value.

41. (Original) The method of claim 35, wherein the second signal is a reset signal.

42. (Original) The method of claim 41, wherein the reset signal is generated in response to a clock signal having a frequency that fails to exceed a predetermined minimum value.

43. (Original) The method of claim 42, wherein the reset signal is generated by a monostable circuit.

44. (Currently Amended) A method comprising:

monitoring a data signal to determine whether a data signal condition exists,

wherein a data signal condition exists if the data signal maintains a present data level beyond a predetermined limit wherein monitoring a data signal comprises:

initializing an asynchronous counter;

updating the asynchronous counter when the data signal is maintained for more than one clock cycle;

resetting the asynchronous counter when the data signal is not maintained for more than one clock cycle; and
determining whether the asynchronous counter exceeds a predetermined limit;

generating a power down signal in response to the data signal condition to prevent a DC flow condition;

monitoring a clock signal; and

generating a reset signal in response to a clock signal condition to prevent the DC flow condition.

45. (Previously Presented) The method of claim 44, wherein the data signal is provided by a delta-sigma modulator.

46. (Currently Amended) The method of claim [[41]] 44, wherein a clock signal condition exists if the clock signal has a frequency that fails to exceed a predetermined minimum value.

47. (Canceled)

48. (Previously Presented) The method of claim 44, wherein generating a reset signal comprises generating the reset signal using a monostable circuit.

49. (Currently Amended) A method comprising:

monitoring a data signal, wherein monitoring comprises:

initializing an asynchronous counter;

updating the asynchronous counter when the data signal is

maintained for more than one clock cycle;

resetting the asynchronous counter when the data signal is not

maintained for more than one clock cycle; and

determining that a signal fault condition exists based on the asynchronous counter and a predetermined limit;

generating a power down signal if a signal fault condition exists the data signal maintains a present data level for a predetermined number of clock cycles;

monitoring for an anomalous clock signal comprising a clock signal with a frequency that fails to exceed a predetermined minimum value; and

generating a reset signal if an anomalous clock signal exists.

50. (Previously Presented) The method of claim 49, wherein monitoring for an anomalous clock signal comprises monitoring how long the clock signal remains high

and low.

51. (Previously Presented) The method of claim 50, further comprising monitoring whether the clock signal remains high or low beyond a predetermined limit of time.

52. (Previously Presented) The method of claim 49, wherein generating a reset signal comprises generating the reset signal using a monostable circuit.

53. (Previously Presented) The method of claim 49, wherein monitoring a data signal comprises monitoring a data signal from a delta-sigma modulator.